WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a workpiece;

a first insulating layer formed over the workpiece;

at least one second insulating layer formed over the first insulating layer; and

at least one metal-insulator-metal (MIM) capacitor formed in the first insulating layer and the at least one second insulating layer, the at least one MIM capacitor comprising a first conductive layer, a dielectric layer disposed over the first conductive layer, and a second conductive layer formed over the dielectric layer, and wherein the first conductive layer extends completely to a top surface of the at least one second insulating layer.

2. The semiconductor device according to Claim 1, wherein the first conductive layer and the second conductive layer comprise a refractory metal, TiN, TaN, Ta, TaSiN, TiW, NiCr, MoN, Ru, WN, WSi, Cu, Al, W, Ti, Ta, Co, N, Ni, Mo, other metals, combinations thereof, or polysilicon, and wherein the MIM capacitor is formed in an interconnect layer of the semiconductor device.

3. The semiconductor device according to Claim 1, wherein the dielectric layer comprises Al, Si, O, N, Ti, Ta, lead-zirconate-titanate (PZT), barium strontium titanate (BST), $Ta_2O_5$, $Al_2O_3$, $SiO_2$, or combinations thereof.

4. The semiconductor device according to Claim 1, wherein the at least one second insulating layer comprises 2, 3, 4, 5, or 6 or more insulating layers, wherein the MIM capacitor is formed in the entire thicknesses of the second insulating layers.

5. The semiconductor device according to Claim 4, wherein the workpiece comprises a plurality of elements formed therein, further comprising:

at least one third insulating layer disposed between the workpiece and the first insulating layer; and

at least one conductive region formed in each third insulating layer abutting the first conductive layer of the at least one MIM capacitor, wherein each conductive region and the first conductive layer comprise a bottom plate of the at least one MIM capacitor, and wherein the at least one conductive region makes electrical contact to an element in the workpiece.

6. The semiconductor device according to Claim 5, wherein the at least one third insulating layer comprises a first metallization layer of the semiconductor device, wherein the first insulating layer comprises a first via layer of the semiconductor device, wherein the at least one second insulating layer comprises a second metallization layer of the semiconductor device, and wherein the at least one MIM capacitor is formed in the first via layer and the second insulating layer of the semiconductor device.

7. The semiconductor device according to Claim 5, wherein the at least one third insulating layer comprises a first metallization layer, at least one first via layer and at least one second metallization layer of the semiconductor device, wherein the first insulating layer comprises at least one second via layer of the semiconductor device, wherein the at least one second insulating layer comprises at least one third metallization layer of the semiconductor device, wherein the at least one MIM capacitor is formed in the at least one second via layer and the at least one third insulating layer of the semiconductor device, and wherein a bottom plate of the at least one MIM capacitor comprises the first conductive layer and the conductive regions in the third insulating layer.

8. The semiconductor device according to Claim 1, wherein the at least one MIM capacitor comprises an array of memory devices, the array having a dimension of 2x1 or greater.

9. The semiconductor device according to Claim 1, wherein the first conductive layer comprises a bottom electrode, the dielectric layer comprises a capacitor dielectric, and the second conductive layer comprises a top electrode, wherein the bottom electrode, top electrode, or both are formed by a chemical-mechanical polish (CMP) process.

10. The semiconductor device according to Claim 1, wherein the MIM capacitor is formed in a stand-alone memory device, embedded memory device, non-voltage memory device, ferro-electro memory device, magneto-electro memory device, static random access memory (SRAM) device, dynamic random access memory (DRAM) device, digital device, RF device, analog device, or mixed-mode device.

11. The semiconductor device according to Claim 1, wherein the workpiece comprises a first region and a second region, wherein the at least one MIM capacitor is formed over the first region, further comprising conductive regions formed in the first insulating layer and the second insulating layer over the second region of the workpiece.

12. The semiconductor device according to Claim 11, wherein the first region comprises a DRAM region, wherein the second region comprises a logic region, and wherein the at least one MIM capacitor comprises a storage node of a DRAM memory cell in the DRAM region.

13. The semiconductor device according to Claim 11, wherein the first insulating layer comprises a via layer of the semiconductor device, wherein the second insulating layer comprises a metallization layer of the semiconductor device, and wherein the conductive regions in the second region comprise a dual damascene structure.

14. The semiconductor device according to Claim 1, wherein the second insulating layer comprises a recessed region between at least two adjacent MIM capacitors, the at least two MIM capacitors having top plates comprised of the second conductive layer, wherein the second conductive layer fills the recessed region of the second insulating layer, electrically coupling together the top plates of at the least two adjacent MIM capacitors.

15. The semiconductor device according to Claim 1, wherein the workpiece comprises a plurality of elements formed therein, further comprising a third insulating layer formed between the workpiece and the first insulating layer, further comprising at least one first conductive region disposed in the third insulating layer abutting the first conductive layer of the at least one MIM capacitor, wherein the at least one first conductive region and the first conductive layer comprise a bottom plate of the at least one MIM capacitor.

16. The semiconductor device according to Claim 15, wherein the at least one first conductive region comprises a conductive barrier layer and a conductive material disposed over the conductive barrier layer.

17. The semiconductor device according to Claim 15, wherein the at least one first conductive region electrically couples the at least one MIM capacitor to an element in the workpiece.

18. The semiconductor device according to Claim 15, wherein the first conductive region and the third insulating layer comprise a first metallization layer of the semiconductor device, wherein the first insulating layer comprises a first via layer of the semiconductor device, wherein the second insulating layer comprises a second metallization layer of the semiconductor device, and wherein the at least one MIM capacitor is formed in the first via layer and the second metallization layer of the semiconductor device.

19. The semiconductor device according to Claim 15, further comprising at least one fourth insulating layer disposed between the first insulating layer and the third insulating layer, and a second conductive region formed in each at least one fourth insulating layer between the first conductive region and the at least one MIM capacitor, wherein the second conductive region electrically couples the at least one MIM capacitor to the first conductive region.

20. The semiconductor device according to Claim 19, wherein the third insulating layer and the first conductive region comprise a first metallization layer of the semiconductor device, wherein the at least one fourth insulating layer and the second conductive region comprise a first via layer and a second metallization layer of the semiconductor device, wherein the first insulating layer comprises a second via layer of the semiconductor device, wherein the second insulating layer comprises a third metallization layer of the semiconductor device, and wherein the at least one MIM capacitor is formed in the second via layer and the third metallization layer of the semiconductor device.

21. The semiconductor device according to Claim 1, wherein the second conductive layer of the MIM capacitor comprises a conductive barrier layer and a conductive material disposed over the conductive barrier layer.

22. A semiconductor device, comprising:

a workpiece;

a first insulating layer formed over the workpiece;

a second insulating layer formed over the first insulating layer;

at least one third insulating layer formed over the second insulating layer; and

at least one metal-insulator-metal (MIM) capacitor formed in the at least one third insulating layer, the second insulating layer, and the first insulating layer, the at least one MIM capacitor comprising a first conductive layer, a dielectric layer disposed over the first conductive layer, and a second conductive layer formed over the dielectric layer.

23. The semiconductor device according to Claim 22, wherein the first insulating layer comprises a first via layer of the semiconductor device, wherein the second insulating layer comprises a first metallization layer of the semiconductor device, wherein the at least one third insulating layer comprises at least one second via layer and at least one second metallization layer of the semiconductor device, wherein the at least one MIM capacitor extends through the entire thicknesses of the first via layer, the first metallization layer, the at least one second via layer, and the at least one second metallization layer.

24. The semiconductor device according to Claim 22, wherein the workpiece comprises a plurality of elements formed therein, further comprising:

at least one fourth insulating layer disposed between the workpiece and the first insulating layer; and

at least one conductive region formed in each fourth insulating layer between the first conductive layer of the at least one MIM capacitor and an element in the workpiece, wherein each conductive region and the first conductive layer comprise a bottom plate of the at least one MIM capacitor.

25. The semiconductor device according to Claim 24, wherein the at least one fourth insulating layer comprises a first metallization layer of the semiconductor device, wherein the first insulating layer comprises a first via layer of the semiconductor device, wherein the second insulating layer comprises a second metallization layer of the semiconductor device, wherein the at least one third insulating layer comprises at least one second via layer and at least one third metallization layer of the semiconductor device, and wherein the at least one MIM capacitor extends through the entire thicknesses of the first via layer, the second metallization layer, the at least one second via layer, and the at least one second metallization layer.

26. The semiconductor device according to Claim 22, wherein a top at least one third insulating layer comprises a recessed region between at least two adjacent MIM capacitors, the at least two MIM capacitors having top plates comprised of the second conductive layer, wherein the second conductive layer fills the recessed region of the top at least one third insulating layer, electrically coupling together the top plates of at the least two adjacent MIM capacitors.

27. A semiconductor device, comprising:

a workpiece;

at least one first insulating layer formed over the workpiece; and

a plurality of metal-insulator-metal (MIM) capacitors formed in the at least one first insulating layer, the plurality of MIM capacitors comprising a first conductive layer, a dielectric layer disposed over the first conductive layer, and a second conductive layer formed over the dielectric layer, the second conductive layer comprising a top plate of the plurality of MIM capacitors, wherein a top at least one first insulating layer comprises a recessed region between at least two adjacent MIM capacitors, and wherein the second conductive layer fills the recessed region of the top at least one first insulating layer, electrically coupling together the top plates of the at least two adjacent MIM capacitors.

28. The semiconductor device according to Claim 27, wherein the at least one first insulating layer comprises at least two insulating layers, wherein one first insulating layer comprises a via layer of the semiconductor device, and wherein another first insulating layer comprises an interconnect layer formed over the via layer.

29. The semiconductor device according to Claim 27, wherein the workpiece comprises a plurality of elements formed therein, further comprising at least one second insulating layer formed between the workpiece and the first insulating layer, further comprising a conductive region formed in each at least one second insulating layer, the conductive regions electrically coupling the first conductive layer of the MIM capacitor to an element in the workpiece, wherein the conductive regions and the first conductive layer comprise a bottom plate of the at least one MIM capacitor.

30. The semiconductor device according to Claim 29, wherein the at least one first insulating layer comprises at least two insulating layers, wherein the conductive region and the at least one third insulating layer comprise at least one first metallization layer of the semiconductor device, wherein one first insulating layer comprises a first via layer formed over the at least one first metallization layer, and wherein another first insulating layer comprises a second metallization layer formed over the first via layer.

31. A method of manufacturing a semiconductor device, the method comprising:

providing a workpiece;

depositing a first insulating layer over the workpiece;

depositing at least one second insulating layer over the first insulating layer;

patterning the at least one second insulating layer and the first insulating layer with a pattern for at least one metal-insulator-metal (MIM) capacitor;

depositing a first conductive layer over the patterned at least one second insulating layer and the patterned first insulating layer;

depositing a dielectric layer over the first conductive layer;

depositing a second conductive layer over the dielectric layer; and

removing the second conductive layer, the dielectric layer and the first conductive layer from a top surface of the top at least one second insulating layer, wherein the second conductive layer, the dielectric layer and the first conductive layer in the at least one MIM capacitor pattern comprises at least one MIM capacitor, and wherein the first conductive layer extends completely to the top surface of the top at least one second insulating layer.

32. The method according to Claim 31, wherein the workpiece comprises a first region and a second region, wherein patterning the second insulating layer and the first insulating layer with a pattern for the at least one MIM capacitor comprises patterning the second insulating layer and the first insulating layer over the first region, further comprising:

forming conductive regions in the first insulating layer and the second insulating layer over the second region of the workpiece using a damascene process, wherein depositing the second conductive layer comprises forming the conductive regions over the second region of the workpiece.

33. The method according to Claim 31, further comprising, after depositing the first conductive layer over the patterned second insulating layer and the patterned first insulating layer, removing the first conductive layer and recessing the second insulating layer in a region over a portion of at least two MIM capacitor patterns, wherein depositing the second conductive layer comprises filling the recessed second insulating layer, forming at least two MIM capacitors having top plates that are electrically coupled together.

34. The method according to Claim 31, wherein the workpiece comprises a plurality of elements formed therein, further comprising forming at least one third insulating layer between the workpiece and the first insulating layer, further comprising forming a first conductive region in each third insulating layer, wherein the at least one first conductive region and the first conductive layer comprise a bottom plate of the at least one MIM capacitor, and wherein the at least one first conductive region electrically couples the at least one MIM capacitor to an element in the workpiece.

35. A method of manufacturing a metal-insulator-metal (MIM) capacitor, the method comprising:

providing a workpiece;

depositing a first insulating layer over the workpiece;

depositing a second insulating layer over the first insulating layer;

depositing at least one third insulating layer over the second insulating layer;

patterning the at least one third insulating layer, the second insulating layer and the first insulating layer with a pattern for at least one MIM capacitor;

depositing a first conductive layer over the patterned second insulating layer and the patterned first insulating layer;

depositing a dielectric layer over the first conductive layer;

depositing a second conductive layer over the dielectric layer; and

removing the second conductive layer, the dielectric layer and the first conductive layer from a top surface of the at least one third insulating layer, wherein the second conductive layer, the dielectric layer and the first conductive layer in the at least one MIM capacitor pattern comprises at least one MIM capacitor.

36. The method according to Claim 35, wherein the workpiece comprises a first region and a second region, wherein patterning the at least one third insulating layer, the second insulating layer and the first insulating layer with a pattern for the at least one MIM capacitor comprises patterning the at least one third insulating layer, the second insulating layer and the first insulating layer over the first region, wherein depositing the second conductive layer comprises forming conductive regions over the second region of the workpiece.

37. The method according to Claim 35, further comprising, after depositing the first conductive layer over the at least one third insulating layer, the patterned second insulating layer, and the patterned first insulating layer, removing the first conductive layer and recessing a top third insulating layer in a region over a portion of at least two MIM capacitor patterns, wherein depositing the second conductive layer comprises filling the recessed second insulating layer, forming at least two MIM capacitors having top plates that are electrically coupled together.

38. The method according to Claim 35, wherein the workpiece comprises a plurality of elements formed therein, further comprising forming at least one fourth insulating layer between the workpiece and the first insulating layer, further comprising forming a conductive region in each fourth insulating layer, wherein the conductive region provides electrical connection between an element in the workpiece and the first conductive layer of the at least one MIM capacitor, wherein the conductive region and the first conductive layer comprise a bottom plate of the at least one MIM capacitor.

39. The method according to Claim 35, wherein the MIM capacitor is formed in a stand-alone memory device, embedded memory device, non-voltage memory device, ferro-electro memory device, magneto-electro memory device, static random access memory (SRAM) device, dynamic random access memory (DRAM) device, digital device, RF device, analog device, or mixed-mode device.

40. The method according to Claim 35, wherein depositing the at least one third insulating layer comprises depositing 2, 3, 4, 5, or 6 insulating layers.

41. The method according to Claim 35, wherein depositing the first conductive layer and the second conductive layer comprises depositing Si, Al, Cu, W, Ti, Ta, Co, N, Ni, Mo, Ru, other metallic materials, or combinations thereof, and wherein depositing the dielectric layer comprises depositing Al, Si, O, N, Ti, Ta, lead-zirconate-titanate (PZT), barium strontium titanate (BST), $Ta_2O_5$, $Al_2O_3$, $SiO_2$, other dielectric materials, or combinations thereof.

42. A method of manufacturing a semiconductor device, the method comprising:

providing a workpiece, the workpiece comprising a first region and a second region and having elements formed therein;

depositing a first insulating layer over the workpiece;

forming a plurality of first conductive regions in the first insulating layer over at least the first region of the first insulating layer, the first conductive regions making electrical contact with elements in the workpiece;

depositing a second insulating layer over the first insulating layer and the first conductive regions;

depositing at least one third insulating layer over the second insulating layer;

patterning the at least one third insulating layer and the second insulating layer with a pattern for a plurality of metal-insulator-metal (MIM) capacitors over the workpiece first region, exposing the first conductive regions;

depositing a first conductive layer over at least a top third insulating layer, the second insulating layer and the exposed first conductive regions;

removing the first conductive layer and a top portion of the top third insulating layer in a region between at least two adjacent MIM capacitor patterns, leaving a portion of the top third insulating layer recessed;

depositing a dielectric layer over the first conductive layer and the recessed top third insulating layer;

depositing a second conductive layer over the dielectric layer; and

removing the second conductive layer, the dielectric layer and the first conductive layer from a top surface of the top third insulating layer, wherein the second conductive layer, the

dielectric layer and the first conductive layer in the at least one MIM capacitor pattern comprises at least one MIM capacitor, and wherein depositing the second conductive layer comprises filling the recess in the top third insulating layer, coupling together the top plates of the at least two adjacent MIM capacitors.

43. The method according to Claim 42, wherein removing the first conductive layer and a top portion of the top third insulating layer in a region between at least two MIM capacitor patterns comprises:

depositing a photoresist;

removing a top portion of the photoresist from the region between the at least two adjacent MIM capacitor patterns, exposing portions of the first conductive layer;

etching away exposed portions of the first conductive layer and the top portion of the third insulating layer; and

removing the photoresist.

44. The method according to Claim 42, wherein removing the second conductive layer, the dielectric layer and the first conductive layer from a top surface of the second insulating layer comprises a chemical-mechanical polish (CMP) process.